



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,755	10/22/2003	Barton E. Bennett	OTC0001	5377
27187	7590	03/26/2007	EXAMINER	
BAKER & DANIELS LLP			NGUYEN, HOA CAO	
205 W. JEFFERSON BOULEVARD			ART UNIT	PAPER NUMBER
SUITE 250			2841	
SOUTH BEND, IN 46601				
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MONTHS	03/26/2007	PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/690,755	BENNETT, BARTON E.
	Examiner	Art Unit
	Hoa C. Nguyen	2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 22 December 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) 12-21 and 23-30 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-11, 22, 31 and 34-36 is/are rejected.
- 7) Claim(s) 32-33 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 15-20 and 23-30 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention group, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 12/22/06, in which Species 5 was elected and that, in according to the applicant, claims 1-14, 21-22, and 31-36 read on the elected Species 5 (figures 11-13).

Claims 12-14 contain a limitation (heat sink lead) that does not disclose in the structure shown in Species 5. Therefore, claims 12-14 are not considered in this Office action.

Claim 21 contains a limitation (a larger structure composite structure) that does not disclose in the structure shown in Species 5. Therefore, claim 21 is not considered in this Office action.

Therefore, only claims 1-11, 22, and 31-36 are treated on the merits in this Office action.

Claim Objections

2. Claim 32 is objected to because of the following informalities: The "at lease" must be changed to "at least". Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-11, 22, 31, and 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dibene, II et al. (US 6304450, hereafter Dibene) in view of McClanahan et al. (US 5396397, hereafter McClanahan).

Regarding claim 1, as shown in figures 1 and 2, Dibene discloses a composite sandwich structure with embedded electronics (an encapsulated circuit assembly, see abstract) comprising:

(a) First and second multilayer printed circuit board 102 and 104 (col.3:24-43), each conventionally having a plurality of dielectric laminates (col.1:22-27, wherein a selected number of layers can be arbitrarily considered as facesheet laminates);
(b) a core structure 122/141/120/142 (spacer/fastener, col.3:54 and col.4:7); and
(c) electronic components 108-116/302-308 (devices, col.3:33 and col.4:49) located in a central region where the core structure is located and inherently having electrical conducting pins (conventional surface plug-in components for example) in contact with and secured to the printed circuits within either of the multilayer PCB 102/104.

But, Dibene fails to disclose the first and the second PCB 102/104 in which each containing multilayer composite facesheet laminates made of structural fiber reinforced material and first and second multilayer circuit laminates made of low dielectric constant fiber reinforced material with electrically conducting circuits embedded between low dielectric plies.

The Examiner takes Official Notice that circuit boards having dielectric substrate made of structural fiber reinforced material are old and well known in the art. And, it is noted that applicant also admitted that the structural fiber reinforced material (including low dielectric property) is commonly known in the art (see Specification, par.3-4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the first and the second PCB 102/104 made of structural fiber reinforced material. Since, this feature is well known in the printed circuit board art.

McClanahan, as shown in figures 1-8, teaches a multilayer circuit board having high and low dielectric property regions (different dielectric constant regions, see abstract) in which wiring patterns 7 (col.32-53, figure 1 also see figure 6 col.6:19-35) are formed in the low dielectric region in order to minimize EMI effects (col.3:37 continuing to col.4:5).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings about the minimizing EMI effects from McClanahan on the circuit boards 102/104 of Dibene to have low dielectric property layers, where the devices 108-116 and 302-308 are mounted, having electrical conducting printed circuits embedded therein between in order to minimize EMI effects in high frequency operations.

Regarding claims 2-5, Dibene does not disclose reinforce materials or any of ceramic, glass, composite material, polymere material, polymide, teflon, woven, or non-woven dielectric material.

The Examiner takes Office Notice that reinforced composite materials containing any of ceramic, glass, composite material, polymere material, polyimide, teflon, woven, or non-woven dielectric material are old and well known in the art.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the first and the second PCB 102/104 made of any of the above structural fiber reinforced material. Since, this feature is well known in the printed circuit board art.

Regarding claim 6, as shown in figure 1A, Dibene discloses the first and second multilayer circuit laminates that are located on opposite sides of the core structure, and the multilayer circuit laminates and the core structure are sandwiched between the first and second multilayer composite facesheet laminates.

Regarding claims 7-9, as shown in figure 1A, Dibene discloses the first multilayer composite facesheet laminate which is inherently bonded to the first multilayer circuit laminate, and the second multilayer composite facesheet laminate is inherently bonded to the second multilayer circuit laminate.

Regarding claims 10-11, Dibene discloses every limitation as shown in claim 1 above but failed to disclose the redundant circuitry and components and a signal control device to sense if the equivalent components of circuitry have malfunctioned or failed and a switch to electronically reconfigure the circuitry to isolate the equivalent components or circuitry that have malfunctioned or failed and activate the redundant circuitry and components.

The Examiner takes Official Notice that an electronic device/system having redundant circuitry and its components build therein is merely a matter of design choice in minimizing down time operations.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have a redundant circuitry and components which are activated if equivalent components or circuitry malfunctioned or failed in order to prevent down time operations. Since, this feature is well known in the art.

Furthermore, the limitation regarding the redundant circuitry and components and a signal control device to sense if the equivalent components of circuitry have malfunctioned or failed and a switch to electronically reconfigure the circuitry to isolate the equivalent components or circuitry that have malfunctioned or failed and activate the redundant circuitry and components is interpreted to only require the ability to so perform. In the case of product claim, only the structure of the claim distinguishes over the prior art.

Regarding claim 22, as shown in figure 1A, Dibene discloses the core structure is porous and the electronic components are embedded in the porous core structure.

Regarding claim 31, as shown in figure 1A, Dibene discloses the core structure includes truss elements 120/122/141/142 (considering these elements support the sandwich structure).

Regarding claim 34-36, as shown in figure 1A, Dibene discloses the truss elements have angled structure member (90 degrees angle), and the truss elements can be discreetly attached and arranged in a desired array between the first and the

second multilayer circuit laminates, and the truss elements extend only partially across the length of the composite sandwich structure.

Allowable Subject Matter

5. Claims 32 and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for allowance

6. The following is an examiner's statement of reasons for allowance: The best prior references art of record, taken alone or in combination, fails to teach or fairly suggest a circuit layer attached to the truss elements (claim 32), or at least some of the electronics components are mounted on and electrically connected to the circuit layer on the truss elements (claim 33).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hoa C. Nguyen
3/16/07

Dean A. Reichard
DEAN A. REICHARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800
3/20/07